REMARKS

Claims 1-41 are pending in this application. Claims 11-18 and 30-39 have been withdrawn from consideration and claims 1-10, 19-29, and 40-41 have been rejected. The claims have been amended as indicated above with support for the amendments in paragraphs [11] and [32] of the specification.

Rejection under 35 U.S.C. § 112, ¶ 1

The Office has rejected claims 40 and 41 under 35 U.S.C. § 112, ¶ 1 as containing non-enabled subject matter, e.g., the Office alleges that the present application shows a thick gate insulator 170 in Figure 2 and discloses a gate insulator but claims 40 and 41 recite a transistor without a gate insulator. Applicant respectfully traverses this rejection for the reasons of record. Nevertheless, in an effort *solely* to expedite prosecution, Applicant has amended claims 40 and 41 as indicated above. Thus, Applicant respectfully requests withdrawal of this rejection.

Rejection under 35 U.S.C. § 112, ¶ 2

The Office has rejected claims 1-10 and 19-20 under 35 U.S.C. § 112, ¶2 as being indefinite for the reasons noted on page 2. Applicant respectfully traverses this rejection.

Definiteness is not analyzed in a vacuum, but in light of the teachings of the specification, the teachings of the prior art, and the interpretation given to the claims by the skilled artisan. *See M.P.E.P. § 2173.02.* The teachings of the specification as to a thin and thick gate oxide layer have been made of record. The teachings of the prior art and the skilled artisan's interpretation

are particularly important to whether the Office has substantiated that the rejected claims are indefinite.

The undersigned performed a search for issued patents since 1976 on the Office web site for claims containing the word "semiconductor" and the term "thin gate oxide layer" (search parameters [aclm/semiconductor and "thin gate oxide layer"]). That search uncovered 42 hits, meaning that 42 patents since 1976 that have issued for a semiconductor device containing a "thin gate oxide layer" phrase in the claims. Those 42 patents included U.S. Patent No. 6,586,306 which contains a claim (1) for making a semiconductor device, including the steps of forming a "thin gate oxide layer" in one region and a "thick gate oxide layer" in another region. *See Exhibit A.* Thus, the Office felt that the term "thin" gate oxide layer was sufficiently definite in at 42 instances to allow claims containing such a phrase.

Applicant did not search on the presumably numerous patents that contain such a phrase in the specification. But based on the sheer number of patents containing such a phrase, the skilled artisan would surely have known what constituted a thin gate oxide layer and would have therefore understood such a phrase to have been definite. Indeed, information that is well known in the art and understood by the skilled artisan should be omitted from the specification. *See, for example, M.P.E.P. § 2164.*

The term "thin" gate oxide layer must be definite since the Office has issued numerous claims containing such a term. It is, therefore, unlikely that the Office can now argue that such a term in now indefinite. As well, such a term would have been understood by the skilled artisan based on its extensive use in the art. Thus, the Office has not shown that the rejected claims would have been indefinite to the skilled artisan and Applicant respectfully requests withdrawal of this rejection.

Rejection under 35 U.S.C. § 102 over Murakami et al.

The Office has rejected claims 1-4, 7-10, 19, 23, 26, 27, and 29 under 35 U.S.C. § 102(b) as being anticipated by Murakami et al. (U.S. Patent No. 5,623,154) for the reasons detailed on pages 3-7 of the Office Action. Applicant respectfully traverses this rejection.

The Office argues that Murakami et al. teach the claimed invention pointing to various components of the device in Figure 1. Applicant respectfully disagrees that the Office has shown that the device in Figure 1 of Murakami et al. describes every limitation in the rejected claims.

The independent claims currently contain the limitation that the transistor has a current path between a source and a drain while containing no thin gate insulating layer. As described in paragraphs [11] and [32] of the specification, the transistor described in the present application contains an inversion layer (135) that provides a current path between the source and drain regions, yet without using a thin gate insulating layer, thereby protecting against ESD stress. The prior art devices (as illustrated in Figure 1) were unable to protect against the ESD stress because the thin gate insulating layer (19) in the transistor would break down. *See paragraphs [7] and [8] of the specification.*

The Office has not shown that Murakami et al. discloses this limitation in the rejected independent claims. This reference discloses an NMOS transistor 20 containing source and drain regions 11, a gate oxide film 15, and a gate electrode layer 17. *See column 1, lines 25-50 and Figure 1.* As recognized by the skilled artisan, the gate oxide film 15 would classify as a thin gate insulating layer. Based on the structure of the NMOS transistor depicted in Figure 1, it would be difficult for the Office to substantiate that Murakami et al. disclose a transistor with the features presently claimed.

Accordingly, the Office has not shown that Murakami et al. teach each and every limitation in the rejected claims and Applicant respectfully requests withdrawal of this ground of rejection.

CONCLUSION

For the above reasons, as well as those of record, Applicant respectfully requests the Office to withdraw the pending grounds of rejection and allow the pending claims.

If there is any fee due in connection with the filing of this Amendment, including a fee for any extension of time not accounted for above, please charge the fee to our Deposit Account No. 50-0843.

Respectfully Submitted,

By _____
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